What is Claimed is:

[c1] Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the LANs, the data transmission system comprising:

a packet switch comprising at least a packet switch module interconnecting the plurality of LAN adapters wherein a packet transmitted by any adapter to the packet switch includes a header containing at least the address of the adapter to which the packet is forwarded, the packet switch module includes a plurality of input ports and a plurality of output ports both being respectively connected to the plurality of LAN adapters, each pair of input and output ports defining a cross point within the packet switch module,

wherein the packet switch comprises a memory block located at each of the cross points, the memory block including a data memory unit for storing at least a data packet and a first memory controller which determines from the header of the received data packet whether the packet is to be forwarded to the output port associated with the cross point and for storing the data packet into the data memory unit in such a case, and a data controller which forwards to the output port a data packet stored in a data memory unit of a memory block corresponding to the output port at each clock time.

[c2] Data transmission system according to claim 1, wherein the data controller includes a scheduler associated with each output port, the scheduler selecting at each clock time a memory block corresponding to the output port and causing the memory block to forward the data packet stored in the data memory unit to the output port when predetermined criteria are met.

[c3] Data transmission system according to claim 2, wherein the memory block includes a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point, and the first memory controller stores the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward it to the output port.

[c4] Data transmission system according to claim 2, further comprising an output data block connected to each output port for storing a data packet received from any memory block and transmitting the data packet to the output port under the control of the scheduler.

[c5] Data transmission according to claim 4, wherein the output data block includes a data selection block for validating the data packet after receiving a validating signal from the scheduler, an output memory unit for storing the data packet, and a second memory controller for controlling the operation of storing the data packet into the output memory unit and the operation of reading the output memory unit for transmitting the data packet to the output port.

[c6] Data transmission system according to claim 2, further comprising an input control block connected to each input port for buffering a data packet received from the input port before transmitting the data packet over a distributed data bus connected to all memory blocks corresponding to the input port.

[c7] Data transmission system according to claim 6, wherein the input control block includes an input memory unit for buffering the data packet received from the input port and a third memory controller which stores the data packet into the input memory unit, and reading the data packet to forward it over the distributed data bus.

[c8] Data transmission system according to claim 7, wherein the input control block further includes a multiplexer for selecting either the output of the input memory unit or directly the bus connected to the input port when the input control block is not a first switch module of a plurality of switch modules.

[c9] Data transmission system according to claim 8, wherein the packet switch includes a plurality of switch modules and wherein each down switch module includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up switch module and corresponding to the same output port as the output port of the down switch module.

[c10] Data transmission system according to claim 9, wherein the input expansion

data block includes an expansion memory unit for buffering the data packet received from the expansion bus in and a fourth memory controller which stores the data packet into the expansion memory unit and reading the expansion memory unit to forward it to the output port of the down switch module.

[c11] Data transmission system according to claim 1, wherein the fourth memory controller sends an overflow signal to the data controller when it has detected that the data memory unit overflows.

[c12] Data transmission system according to claim 11, further comprising an overflow bus to transport the data packet to the data memory unit of another memory block corresponding to the output port after the data controller has prevented the data packet from being stored into the data memory unit which overflows and has selected and validated the data memory unit of another memory block which is not overflowing.

[c13] Data transmission system according to claim 11, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters to request the input adapters to reduce the flow of the data packets transmitted to the packet switch when there is too much overflow detected by one or more of the data controller of the packet switch.

[c14] Data transmission system according to claim 13, further comprising an overflow mechanism adapted to receive overflow control signals from the data controller of the packet switch when there is too much overflow and to transmit an overflow signal to the back-pressure mechanism.

[c15] Data transmission system according to claim 1, wherein the header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when the packet switch comprises several packet switch modules.